REMARKS

The present response is intended to be fully responsive to all points of objection and/or rejection raised by the Examiner and is believed to place the application in condition for allowance. Favorable reconsideration and allowance of the application is respectfully requested.

Applicant asserts that the present invention is new, non-obvious and useful. Prompt consideration and allowance of the claims is respectfully requested.

Status of Claims

Claims 1-17 are pending in the application. Claims 12-17 are withdrawn from consideration. Claims 1-11 have been rejected.

CLAIM REJECTIONS

35 U.S.C. § 102 Rejections

In the Office Action, the Examiner rejected claims 1-5, 7-8, 10 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent No. 4,807,188 (Casagrande).

In addition, the Examiner rejected claims 1-4, 6-8, 10-11 under 35 U.S.C. § 102(b), as being anticipated by U.S. Patent No. 4,992,980 (Park et al.).

Applicant respectfully traverses the Examiner's rejections, because neither one of the cited references is a sufficient reference for showing anticipation of all the limitations recited in independent claim 1. Furthermore, Applicant respectfully believes that the Examiner has misinterpreted the teachings of both cited references while attempting to analogize between their teachings and what is recited in claims limitations of the pending Application. Not only do both references fail to teach or suggest all claim limitations of independent claim 1, but they actually teach away from limitations recited in pending claim 1. More specifically, both cited references fail to teach or suggest the limitation which is recited in claim 1 and pertains

to "...**sensing substantially simultaneously a state of adjacent memory cells through at least a partially shared sensing path**."

Independent claim 1 recites:

1. "A method of reading data in a virtual ground array of memory cells comprising: **sensing substantially simultaneously a state of adjacent memory cells through at least a partially shared sensing path**."

Whereas the Casagrande reference generally teaches:

"An electrically alterable, non volatile memory device capable of enduring a high number of cycles utilizes an array of "semidouble" cells, each formed by a pair of elementary EEPROM cells connected substantially in parallel and a single select transistor. **A special program lines biasing circuit generating a bias voltage representative of a condition wherein one of the two elementary EEPROM structure is broken** and sense amplifiers comprising a comparator circuit comparing the current flowing through an addressed semidouble memory cell with the current flowing through a reference cell comprising a pair of virgin EEPROM type elementary cells **to ensure operability of each bit of the memory also when one of the two elementary cells supporting the bit fails**. Different from known memories, only the EEPROM structure is duplicated while column lines, select lines and ancillary circuitry don't require duplication." (Abstract)

And the Park reference generally teaches:

"A virtual ground electrically programmable read-only memory device in which disturbance to neighboring cells is practically eliminated, is disclosed. In one embodiment the memory device comprises a plurality of memory cells formed in a semiconductor substrate and arranged in rows and columns so as to form an array. During read operations, pairs of adjacent cells are accessed simultaneously by grounding a single column line within the array. **The two adjacent column lines--one on each side of the grounded column line--are coupled to separate read paths**. Within the array, rows of cells store bits from a plurality of data bytes according to a pattern in which pairs of adjacent cells store different bits from different bytes." (Abstract)

As is well established, in order to successfully assert a prima facie case of anticipation, the Examiner must provide a single prior art document that includes every element and limitation of the claim or claims being rejected. Applicant respectfully asserts that the Examiner has failed to establish a prima facie case of anticipation, as neither cited reference teaches or suggests every element and limitation of independent claim 1. More specifically, the Casagrande reference teaches a device in which "*...each memory cell of the device of the invention is composed of two elementary EEPROM cells M1 and M2. The sources of the two elementary EEPROM cells M1 and M2 are connected to a common potential node V.sub.GM of the whole memory array. The control gates of the two elementary EEPROM cells are connected in common to a program line...*" and "*...in case one of the two elementary EEPROM cells is broken, the other may be "written" and "erased" regularly and, above all that the content of the operative elementary cell be correctly readable by an appropriate sense amplifier without interferences caused by the electric current flowing through the broken elementary cell of the pair.*" (Column 4 Lines 4-48). It should be clear to anyone of ordinary skill in the art that what is taught in the above excerpt from the Casagrande reference is fundamentally different from the recited claim limitation of claim 1 which reads "...**sensing substantially *simultaneously* a state of adjacent memory cells through at least a partially shared sensing path.**" While claim 1 of the pending Application recites a method of **substantially simultaneously sensing a state of adjacent memory cells**, the cited reference teaches away from this limitation by teaching a device in which the adjacent cells are actually written and erased independently and each is a backup for the other. The intended function of the device taught in the cited reference is clearly described as providing a backup cell ("virgin") for a damaged cell ("broken").

Regarding the Park reference, the Applicant would like to point the Examiner's attention that the Park reference teaches a device in which "**The two adjacent column lines--one on each side of the grounded column line--are coupled to separate read paths.**" As shown above, the cited reference actually teaches away from the limitation of pending claim 1 that recites "...**sensing substantially simultaneously a state of adjacent memory cells through *at least a partially shared sensing path*.**" While claim 1 of the pending Application recites a method in which the adjacent memory cells have an **at least partially shared**